

 INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)				ATTY DOCKET NO. ITO.0544US (P15589)	SERIAL NO. 10/633,886	
				APPLICANT(S): CHARLES H. DENNISON		
				FILING DATE: August 4, 2003	GROUP ART UNIT:	
U.S. PATENT DOCUMENTS						
*EXAMINER'S INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
A.						
B.						
C.						
D.						
FOREIGN PATENT DOCUMENTS						
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
E.						
F.						
G.						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
<i>Loke</i>	H.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19 th IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003				
<i>Loke</i>	I.	Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change, RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003				
<i>Loke</i>	J.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003				
<i>Loke</i>	K.	Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee, K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003				
<i>Loke</i>	L.	Chieng, C., Lee, J.W., Kersey, P., U.S. Patent Application Serial No. 09/745,835, filed December 21, 2000 entitled "Metal Structure for a Phase-Change Memory Device" <i>6569705</i>				
	M.					
	N.					
EXAMINER	<i>Loke</i>		DATE CONSIDERED	<i>11/13/04</i>		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						